AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An active pixel sensor, comprising:

a plurality of pixels, wherein each of said pixels comprises:

a ~~reset~~ circuit portion for supplying a reset signal and a photosensor charge accumulation signal to a column line ~~resetting a photosensitive element of said pixel~~;

a first storage circuit for receiving said reset signal from said column line and storing [[a]] said reset signal, ~~voltage level of said photosensitive element, wherein~~ said first storage circuit comprising ~~further comprises a first sample and hold circuit, wherein said first sample and hold circuit comprises~~ a first sample and hold transistor switchably coupling a first terminal of a first storage capacitor with said column line ~~reset portion~~; and

a second storage circuit for receiving said photosensor charge accumulation signal from said column line and storing said photosensor charge accumulation signal, ~~a voltage level of said photosensitive element after an integration period, wherein~~ said second storage circuit comprising ~~comprises a second sample and hold circuit, wherein said second sample and hold circuit comprises~~ a second sample and hold transistor switchably coupling a first terminal of a second storage capacitor with said ~~reset portion~~ column line,

wherein said first and second storage circuits are configured to provide the signals respectively stored therein to said column line during a readout operation.

2. (Currently Amended) The active pixel sensor of claim 1, wherein said ~~photosensitive element~~ photosensor charge accumulation signal is generated by a photodiode.

Claims 3-5. (Canceled)

6. (Currently Amended) The active pixel sensor of claim 1, wherein said first terminal of said first storage capacitor is coupled to a gate of a first source follower transistor, a first source/drain terminal of said first source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said first source follower transistor is switchably coupled to said column [[bus]] line.

Claims 7-8. (Canceled)

9. (Currently Amended) The active pixel sensor of claim 1, wherein said first terminal of said second storage capacitor is coupled to a gate of a second source follower transistor, a first source/drain terminal of said second source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said second source follower transistor is switchably coupled to said column [[bus]] line.

Claims 10-16. (Canceled)

17. (Currently Amended) A semiconductor chip, comprising:

an active pixel sensor, said active pixel sensor comprising:

a plurality of pixels, ~~wherein~~ each of said pixels ~~comprises~~ comprising:

a ~~reset~~ circuit portion for supplying a reset signal and a photosensor charge accumulation signal to a column line ~~resetting a photosensitive element of said pixel~~;

a first storage circuit for receiving said reset signal from said column line and storing [[a]] said reset signal, ~~voltage level of said photosensitive element, wherein~~ said first storage circuit comprising ~~further comprises a first sample and hold circuit, wherein said first sample and hold circuit comprises~~ a first sample and hold transistor switchably coupling a first terminal of a first storage capacitor with said ~~reset portion~~ column line; and

a second storage circuit for receiving said photosensor charge accumulation signal from said column line and storing said photosensor charge accumulation signal, ~~a voltage level of said photosensitive element after an integration period, wherein~~ said second storage circuit comprising ~~comprises a second sample and hold circuit, wherein said second sample and hold circuit comprises~~ a second sample and hold transistor switchably coupling a first terminal of a second storage capacitor with said ~~reset portion~~ column line,

wherein said first and second storage circuits are configured to provide the signals respectively stored therein to said column line during a readout operation.

18. (Currently Amended) The semiconductor chip of claim 17, wherein said photosensor charge accumulation signal ~~photosensitive element~~ is generated by a photodiode.

Claims 19-21. (Canceled)

22. (Currently Amended) The semiconductor chip of claim 17, wherein said first terminal of said first storage capacitor is coupled to a gate of a first source follower transistor, a first source/drain terminal of said first source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said first source follower transistor is switchably coupled to said column [[bus]] line.

Claims 23-24. (Canceled)

25. (Currently Amended) The semiconductor chip of claim 17, wherein said first terminal of said second storage capacitor is coupled to a gate of a second source follower transistor, a first source/drain terminal of said second source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said second source follower transistor is switchably coupled to said column [[bus]] line.

Claims 26-32. (Canceled)

33. (Currently Amended) A processor system, comprising:

a processor; and

an imager device coupled to said processor for sending signals to said processor, said imager device comprising:

a plurality of pixels, ~~wherein~~ each of said pixels comprising ~~comprises~~:

a circuit ~~reset~~ portion for supplying a reset signal and a photosensor charge accumulation signal to a column line ~~resetting a photosensitive element of said pixel~~;

a first storage circuit for receiving said reset signal from said column line and storing [[a]] said reset signal, ~~voltage level of said photosensitive element, wherein~~ said first storage circuit comprising ~~further comprises a first sample and hold circuit, wherein said first sample and hold circuit comprises~~ a first sample and hold transistor switchably coupling a first terminal of a first storage capacitor with said ~~reset portion~~ column line; and

a second storage circuit for receiving said photosensor charge accumulation signal from said column line and storing said photosensor charge accumulation signal, ~~a voltage level of said photosensitive element after an integration period, wherein~~ said second storage circuit comprising ~~comprises a second sample and hold circuit, wherein said second sample and hold circuit comprises~~ a second sample and hold transistor switchably coupling a first terminal of a second storage capacitor with said ~~reset portion~~ column line,

wherein said first and second storage circuits are configured to provide the signals respectively stored therein to said column line during a readout operation.

34. (Currently Amended) The processor system of claim 33, wherein said photosensor charge accumulation signal ~~photosensitive element~~ is generated by a photodiode.

Claims 35-37. (Canceled)

38. (Currently Amended) The processor system of claim 33, wherein said first terminal of said first storage capacitor is coupled to a gate of a first source follower transistor, a first source/drain terminal of said first source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said first source follower transistor is switchably coupled to said column [[bus]] line.

Claims 39-40. (Canceled)

41. (Currently Amended) The processor system of claim 33, wherein said first terminal of said second storage capacitor is coupled to a gate of a second source follower transistor, a first source/drain terminal of said second source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said second source follower transistor is switchably coupled to said column [[bus]] line.

Claims 42-48. (Canceled)

49. (Currently Amended) A method [[for]] of operating an active pixel sensor, the method comprising:

resetting a photosensitive element of a pixel ~~within a reset portion~~, ~~wherein~~ said pixel ~~comprises~~ comprising a circuit portion, a first storage circuit and a second storage circuit;

transferring a reset signal from the circuit portion to a column line;

receiving the reset signal from the column line at the first storage circuit;

storing [[a]] said reset signal ~~voltage of said photosensitive element~~ within said first storage circuit, ~~wherein~~ said first storage circuit comprising ~~comprises a first sample and hold circuit, wherein said first sample and hold circuit comprises~~ a first sample and hold transistor switchably coupling a first terminal of a first storage capacitor with said ~~reset portion~~column line;

exposing said photosensitive element to a light source during an integration period while said reset ~~voltage~~ signal is stored within said pixel; ~~and~~

transferring a charge accumulation signal from the circuit portion to a column line;

receiving the charge accumulation signal from the column line at the second storage circuit;

storing within said second storage circuit [[a]] said charge accumulation signal ~~voltage level of said photosensitive element~~ after said integration period, said reset ~~voltage~~ signal still being stored within said first storage circuit, ~~wherein~~ said second storage circuit comprising ~~comprises a second sample and hold circuit, wherein said second sample and hold circuit comprises~~ a second sample and hold transistor switchably coupling a first terminal of a second storage capacitor with said ~~reset portion~~ column line; and

reading out said reset signal on said column line.

50. (Currently Amended) The method of claim 49 further comprising:

~~reading out said reset voltage from said pixel;~~

reading out said voltage level of said photosensitive element after said integration period; and

generating a difference signal corresponding to a level of light to which said photosensitive element was exposed during said integration period.

Claim 51-53. (Canceled)